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SP605 Master UCF. The UCF template is provided for designs that target the SP605. Net names provided in the constraints below correlate with net names on the SP605 rev. C schematic. On identifying the appropriate pins, the net names below should be replaced with net names in the

user RTL. See the Constraints Guide for more information.

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### **AXI Interface Based ML605/SP605 MicroBlaze Processor Subsystem**

The 'documentation' in this case is the SP605 Hardware User Guide UG526. We (me, at least) are easily confused in this forum, so please don't spare essential details. simply says 667 Mb/s memory bandwidth, which would be 83 MBytes / sec by some logic . A more correct specification is 667 MTransfers/sec.

### **Solved: SP605 SDRAM Bandwidth - Community Forums**

Figure 1-24: FPGA Mode DIP Switch SW1 References For more information, refer to the Spartan-6 FPGA Configuration User Guide [Ref 2]. See Table 1-30, page 55 for the configuration modes. SP605 Hardware User Guide [www.xilinx.com](http://www.xilinx.com) UG526 (v1.1.1) February 1, 2010... Page 50: Vita 57.1 Fmc Lpc Connector

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### **SP605: I2C address of M24C08 EEPROM (U4 ... - forums ...**

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SP605 board configuration. Xilinx UG526 document also known as SP605 Hardware User Guide is your best friend if you want to know more details about usage and configuration of this nice board. To load bitstream from onboard SPI flash chip you need to configure SP605 by turning SW1 switches into the 1-ON, 2-OFF position.

### **GitHub - Cr4sh/s6\_pcie\_microblaze: PCI Express DIY hacking ...**

SPI pins are equivalent on both boards (SP601 and SP605), I changed INIT\_B and DONE using SP605 Hardware User Guide: So yes, INIT\_B is connected to pin 1 on resistor R69. For the pins on the FX3 device I used the following schematic (Because the table states pins number of J7). However I didn't check it was GPIO[52] and so on.

### **Configuring an SP605 Over USB Using Cypress EZ ...**



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